UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/398,913	09/14/1999	ILYA KLEBANOV	0100.9900680	1646

29153 7590 08/09/2007

ADVANCED MICRO DEVICES, INC.
C/O VEDDER PRICE KAUFMAN & KAMMHOLZ, P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
HOYE, MICHAEL W	
ART UNIT	**PAPER NUMBER**
2623	

MAIL DATE	DELIVERY MODE
08/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/398,913	KLEBANOV ET AL.	
	Examiner	Art Unit	
	Michael W. Hoye	2623	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-16 and 18-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2-13,22 and 23* is/are allowed.

6)☒ Claim(s) *14-16,18-21,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/12/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicants' arguments filed on May 23, 2007, with respect to claims 14-16, 18-21 and 24-25, have been fully considered but they are not persuasive.

Regarding claims 14-16 and 24-25, the Applicants' argue beginning on the bottom of page 9 that, "Cheney does not teach a frame buffer that stores both uncompressed data and compressed data from the transport stream in different modes of operation. In fact, it appears that instead Cheney teaches a system that employs frame buffers that store decoded video data in full frame format or a combination of decoded full frame format and scaled decoded video for output to a display as noted, for example, in column 9, lines 26-31. Also, column 9, lines 31-54 specifically state that the encoded streams which is a coded MPEG-2 video data is "fed through memory control unit 652 as coded MPEG-2 video data to the input of video decoder 654." (emphasis added). As such, Cheney teaches that the encoded or compressed video data goes to the video decoder 654 through the memory controller 652 and not into the frame buffer until it is decoded."

In response, and after further consideration, the Examiner respectfully disagrees with the Applicants because given the broadest reasonable interpretation of the claims, the scope of the claimed "compressed transport data" could be considered "previously compressed transport steam data" stored in the memory as disclosed in the Cheney reference as described above in the sections cited by the Applicants as well as in the sections of Cheney discussed in the rejection below. In any future correspondence from the Applicants, the Examiner would kindly appreciate

further clarification and support of how the Applicants claimed invention processes the "compressed transport stream data" (i.e. if the "compressed transport stream data" is stored in a memory (frame) buffer before being processed by a decoder.

Regarding claim 25, the Applicants reassert the remarks made above with respect to claim 14, and the Examiner respectfully disagrees with the Applicants in view of the response to the Applicants' remarks made above with respect to claim 14. In addition, the Applicants argue on page 11 that, "claim 25 includes specific information provided by the secondary control signals, namely as noted in claim [2]5, a start of active frame control signal indicating the first part of the transport stream packet, and end of active frame control signal and so on. The office action does not address this frame based language in the cited portion and the Newton's Telecom Dictionary does not identify any such secondary control signal derived from compressed transport stream control signals that provide such information or the use of such start of active frame control signal information as claimed."

In response, the Examiner respectfully disagrees with the Applicants because Cheney clearly teaches "generating a secondary set of control signals from a compressed transport stream" as shown in Fig. 6 and described in col. 9, line 9 – col. 13, line 36, where an MPEG input source signal is received at the memory control unit 652 and numerous control signals, which include at least the claimed "secondary set of control signals...", are generated from the compressed transport stream or MPEG input source and memory control unit, and wherein "storing at least a portion of the compressed transport stream data signals via a first bus in a memory buffer controlled by the secondary set of control signals" is also met by Fig. 6 and the section cited above of the Cheney reference, where data is stored in via a bus in the frame buffer

memory 653. More specifically, regarding the Applicants argument that, "[the] frame based language in the cited portion and the Newton's Telecom Dictionary does not identify any such secondary control signal derived from compressed transport stream control signals that provide such information or the use of such start of active frame control signal information as claimed." The Examiner respectfully disagrees with the Applicants because, as previously stated, the Cheney et al reference clearly teaches the claimed limitations of claim 25, as described in col. 9, line 9 – col. 13, line 36, as well as in USPN 5,668,599 by Cheney et al., entitled "Memory Management For An MPEG-2 Compliant Decoder," the entirety of which is incorporated by reference (see col. 12, lines 38-42 of USPN 6,519,283). More specifically, as previously stated above for claim 14, Cheney explicitly teaches the use of various types of control signals and/or synchronization signals as described in col. 9, line 9 – col. 13, line 36. Furthermore, the *Newton's Telecom Dictionary* specifically states in the definition of the term "packet" on page 546 that, "...A packet consists of the data to be transmitted and certain **control** information. The three principal elements of a packet include: 1. Header – control information such as synchronizing bits, address of the destination or target device, address of originating device, length of packet, etc. 2. Text or payload – the data to be transmitted... 3. Trailer – end of packet, and error detection and correction bits..." Therefore, the Cheney references clearly indicate that the secondary set of control signals from the compressed transport stream's control signals indicates at least a first byte of a transport stream packet to be stored in the frame buffer, a first byte of the transport stream packet and a last byte of the transport steam packet, as well as error detection and correction bits, which are required in order to process the transport stream

packets/frames and store the packets/frames in a frame buffer memory, and indicate invalid bytes present in the compressed transport stream.

In addition to, the claimed "wherein the memory buffer comprises a frame buffer that stores uncompressed data in a different mode of operation" is met by the frame buffer as described above in response to claim 14, which stores both compressed and uncompressed data in different modes of operation, including both normal and scaled modes of operation (see col. 9, line 9 – col. 13, line 36).

Regarding claims 18-20, the Applicants argue beginning on page 11 that, "There does not appear to be any cite to any reference that teaches such a video graphics adapter that includes a graphics engine and multiple ports as claimed."

In response, the Examiner respectfully disagrees with the Applicants because as previously stated prior Office Actions, as well as in the rejection below:

> The claimed "video graphics adapter..." is met by the video graphics adapter (VGA) 318, as shown in Fig. 5, where the controller 510 or tuner 526 and/or decoder 530 send the MPEG encoded video stream to the MPEG-2 decoder 512 (col. 11, line 34 – col. 12, line 18). The claimed "video graphics adapter further includes a bus interface port coupleable to a central processing unit" is met by the PCI bus interface port from controller 510 in VGA card 318 (see Fig. 5 and col. 11, lines 35-38), which is coupleable to processor 310 via the PCI Bus (see Fig. 3 and col. 9, lines 17-24). The claimed VGA further includes an engine, or graphics engine...is met by the MPEG-2 decoder 512 in Fig. 5, which decompresses the MPEG transport stream (see col. 11, lines 37-44), and the claimed video output port is met by either the audio video output connector 542 (see col. 11, lines 61-63 and col. 12, lines 3-6), or the video output 522 as shown in Fig. 5 (see col. 11, lines 40-55, more specifically lines 52-55). The Schindler et al reference teaches that the digital video broadcast signal as described above is transmitted through the PCI bus 312. Schindler also teaches that the VGA 318 as shown in Fig. 5 may also directly receive broadcast signals through audio and video inputs 524, 544,

> 546 and 548 (col. 11, lines 56-66), more specifically, standard cable connector 524, which may receive broadcasts, is coupled to tuner circuit 526 (col. 11, lines 56-60).

Moreover, as previously stated, "the Schindler et al reference does not explicitly disclose that the video broadcast received through connector 524 is a digital video broadcast, and more specifically the claimed, "transport stream port to receive the compressed transport stream and another transport stream." The So reference was used to provide evidence for that specific claim limitation as noted in the previous Office Action and in the rejection below.

The Applicants argue with regards to the So reference on page 12 that, "the Northbridge chip does not have a graphics engine nor does it include a video output as required by the claim and as such does not qualify as a video graphics adapter."

In response, the Examiner respectfully disagrees with the Applicants' characterization of the rejection in light of the remarks made above, in addition to, the So reference clearly teaches a video graphics adapter 126 directly connected to the North Bridge 108 via 118, as well as multiple video inputs and outputs on P1394, 118 and the PCI bus.

The Applicants further argue on the bottom of page 12 that, "the combination of the references requires the addition of the Northbridge chip 108 which actually increases the cost of the system and requires an additional integrated circuit."

In response, the Examiner respectfully disagrees since the North bridge chip 108 of So actually reduces the number of parts by providing a single integrated interface that is made compliant with whatever suitable specification is desired for each bus as described in col. 131, lines 24-30 of So as stated in the rejection below.

The Applicants also argue on the top of page 13 that, "So teaches away from the combination since the video graphic blocks described do not have the transport steam ports that receive compressed transport stream and another transport stream as well as a bus interface port as claimed but appears to use a conventional video graphics structure."

In response, the Examiner respectfully disagrees because So explicitly teaches in col. 129, lines 22-37, a multimedia system with multiple buses, including a PCI bus or bus 124 in Fig. 1 (330 in later Figs.), as well as the claimed, "transport stream port to receive the compressed transport stream and another transport stream" as met by the north bridge chip 108, which has multiple ports and a PCI or system bus connection through the PCI port to the PCI/system bus 124/330 (see Figs. 1 and 126-127 and col. 129, line 23 – col. 131, line 30). Multiple transport streams may be received through the 1394 port and/or TV tuner 130.

Regarding claim 19, in summary, the Applicants argue on page 13 that, "The office action fails to provide any other reference and any teaching that teaches a graphics memory that stores either data for a graphics engine or stores a compressed transport stream that is coupled to a transport stream port and to a bus interface port as claimed."

In response, the examiner respectfully disagrees because as previously stated, "The So reference as combined above with Schindler [in claim 18] further teaches an internal memory 128 [frame buffer] coupled to the graphics engine 126, the transport stream port (116 of DSP1), and the system bus interface port (PCI 122) to store at least a portion of the transport stream... as previously described above in claim 14."

Regarding independent claim 21, the Applicants' argue on page 14 that, "the cited portion of Schindler refers to decoded video data being placed by the controller into VRAM 518 and again does not refer to a frame buffer that stores either compressed data from a transport stream or uncompressed pixel data for display depending on a mode of operation nor one line/one packet storage structure."

In response the Examiner respectfully disagrees since Schindler teaches that the VGA card is capable of receiving both MPEG encoded video (compressed data), as well as other video input, including NTSC compatible signals (see col. 11, lines 34-62). In addition, the Examiner respectfully disagrees with the Applicants remarks/arguments as quoted above because the Applicants' characterization of the office action is not accurately described, since the Schindler reference was provided in the rejection as evidence of a method of storing video data comprising multiple modes of operation, including receiving uncompressed video data, processing the data and storing the data in a frame buffer memory before sending the video data to the output for display, as well as another mode of operation where compressed transport stream data or an MPEG transport stream is received, processed and stored in a frame buffer memory before being output for display (see relevant sections of the previous Office Action as well as the rejection of claim 21 as described below). Also note the new remarks in this Office Action made above, specifically corresponding to claim 14, which are similarly applied to claim 21. Furthermore, the Examiner respectfully notes that the Maladi reference was used provide evidence of the claimed, "one line of the frame buffer memory is representative of one line of a video image to be displayed", and the Datari reference was used to provide evidence of the claimed, "one line of

the frame buffer memory is representative of one transport stream packet", where the motivation to combine the references has been presented in the rejection.

Claim Objections

2. Claim 25 are objected to because of the following informalities: in line 10 of the claim the claimed "the at least portion" should read --the at least **a** portion--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 14-16 and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheney et al (USPN 6,519,283), in view of So (USPN 5,909,559), both cited by the Examiner.

As to claim 14, note the Cheney et al reference which discloses a method of receiving video graphics data. The claimed "receiving a compressed transport stream associated with a digital video broadcast signal" is met by the digital video from cable or satellite broadcast signal 101 (Fig. 4) received at NIM 102, where a MPEG transport stream is sent to transport logic (XPORT) 103 (see col. 6, line 35-45). The MPEG transport stream is a compressed transport stream. In addition, the claimed "compressed transport stream having data signals and control signals" is inherent to a MPEG transport stream. The Applicants also disclose this in the

"Background of the Invention" (or prior art) section of the specification, which describes the Digital Video Broadcast (DVB) transmission standards and specifically states that, "The compressed MPEG 2 format is referred to as a transport stream. The transport stream from the demodulator comprises a plurality of packets. Each of the transport stream packets comprises one synchronization byte, followed by one of 187 data bytes or 187 data bytes plus 16 extra bytes depending on the format." (See Specification, page 1, lines 15-19), in addition to, it is well known in the art that MPEG transport streams may comprise header information with routing information. Therefore, it is well known in the art that a MPEG transport stream comprises data signals as met by the data bytes, and control signals as met by the synchronization bytes and header information. The claimed "generating a secondary set of control signals from the compressed transport stream's control signals" is met by the video decode system of Figure 6 and is further described in col. 9, line 9 – col. 13, line 36, where an MPEG input source signal is received at the memory control unit 652 and numerous control signals, which include at least the claimed "secondary set of control signals", are generated from the compressed transport stream or MPEG input source and memory control unit, and wherein "storing at least a portion of the compressed transport stream data signals via a first bus in a memory buffer controlled by the secondary set of control signals" is also met by Fig. 6 and the section cited above of the Cheney reference, where data is stored in via a bus in the frame buffer memory 653. In addition to, the claimed "wherein the memory buffer comprises a frame buffer that stores uncompressed data in a different mode of operation" is met by the frame buffer as described above, which stores both compressed and uncompressed data in different modes of operation, including both normal and scaled modes of operation (see col. 9, line 9 – col. 13, line 36). In one example, Cheney teaches

that the MPEG input source is fed through the memory control unit 652 as coded MPEG 2 video data to the input of video decoder 654 and from the Huffman decoder 672 a B picture "MPEG-2 repeat field" signal is sent to display mode switch logic 696 (which also receives a vertical synchronization (VSYNC) signal that is an external synchronization signal) and frame buffer pointer control 686, and from the decoded signals from the MPEG transport stream's control signals, along with other signals, the frame buffer pointer control 686 generates additional control signals (see col. 9, line 31 – col. 12, line 63). More specifically, as described above, a B picture "MPEG-2 repeat field" signal from Huffman decoder 672 of video decoder 654 may be used in part by frame buffer pointer control 686 in Fig. 6 (col. 11, line 5 – col. 12, line 63). The claimed "storing at least a portion of the compressed transport stream data signals via a first bus in a memory buffer controlled by the secondary set of control signals" is also met by the frame buffer pointer control 686, in one mode, controlling the rotation of the frame buffers as described above (also see col. 10, lines 37-41 and col. 11, line 5 – col. 12, line 63), and the clamed "wherein the memory buffer comprises a frame buffer that stores uncompressed data in a different mode of operation", is also met by Cheney where "I pictures" or I frames may be stored in the same memory buffers in both normal and scaled modes of operation (see col. 9, line 9 – col. 13, line 36). Although the Cheney reference discloses a PCI bus 42 (Fig. 2), the Cheney reference does not explicitly disclose the claimed sending the contents of the memory buffer via the first bus to a system bus. The So reference discloses improved integrated circuits and computer system embodiments for desktop and computers, television sets, set-top boxes and appliances improved with asymmetrical multiprocessors (see col. 129, lines 22-37). More specifically, the So reference teaches the use of a multimedia system with multiple buses,

including a PCI bus or bus 124 in Fig. 1 (330 in later Figs.), as well as the claimed, "sending the at least a portion of the compressed transport stream data stored in the memory buffer via a first bus to a system bus" as met by the embedded frame buffer 128 sending the contents of the memory buffer via the AGP bus to the AGP port of the north bridge chip 108, where the contents may be sent to the PCI or system bus 124/330 through the PCI port (see Figs. 1 and 126-127 and col. 129, line 23 – col. 131, line 30). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the method of receiving video graphics data as disclosed by the Cheney et al reference with the teachings the So reference which discloses using a north bridge integrated interface for multiple buses in conjunction with the frame buffer memory and a system or PCI bus for the advantage of having the ability to receive various types of broadcasts or multimedia streams through a computer system with a video graphics adapter or graphics engine and bus type system. One of ordinary skill in the art would have been led to make such a modification since television/multimedia receivers used with computers are well known in the art to provide additional capabilities within a computer system.

As to claim 15, the Cheney reference discloses multiple modes of operation and a method of receiving a digital video signal that is of a different type than the compressed transport stream, which is met by the video signals received at 104 in Fig. 4 (col. 4, lines 40-42 & 54-57 and col. 6, lines 62-67). The Cheney reference discloses a first mode of operation as shown by receiving a digital video signal 101, which includes a compressed MPEG transport stream (col. 6, lines 37-44). The Cheney reference also discloses another mode of operation wherein the digital video signal is of a different type than the compressed transport stream, which is met by the

uncompressed digital video signals received at 104 in Fig. 4 (col. 4, lines 40-42 & 54-57 and col. 6, lines 62-67), which includes data signals including pixel data signals and control signals which are met by the corresponding synchronization signals (col. 4, lines 56-57), and by "pixel select control" signals (col. 7, lines 40-41). The digital multi-standard decoder (DMSD) 105 provides synchronization signals, such as, horizontal sync and vertical sync and the DMSD 105 provides the synchronization signals to the video decoder 106 which interprets the synchronization information and processes the data (col. 7, lines 7-18) to provide a secondary set of control signals through the use of the frame buffer pointer control 686 and other circuitry as shown in the video decode system of Fig. 6 and as previously described above in claim 14.

As to claim 16, the Cheney reference as combined above, further discloses a camcorder or television camera may be used as an uncompressed signal and connected video cameras may inherently comprise the transmission of a zoom video signal (see col. 8, lines 24-25 and ZV port definition from the Microsoft Computer Dictionary, p. 586).

As to claim 24, the Cheney et al reference teaches the claimed limitations of claim 24 as described in col. 9, line 9 – col. 13, line 36 and in USPN 5,668,599 by Cheney et al., entitled "Memory Management For An MPEG-2 Compliant Decoder," the entirety of which is incorporated by reference (see col. 12, lines 38-42 of USPN 6,519,283). More specifically, as previously stated above for claim 14, Cheney explicitly teaches the use of various types of control signals and/or synchronization signals as described in col. 9, line 9 – col. 13, line 36. Furthermore, the *Newton's Telecom Dictionary* specifically states in the definition of the term "packet" on page 546 that, "...A packet consists of the data to be transmitted and certain **control** information. The three principal elements of a packet include: 1. Header – control information

such as synchronizing bits, address of the destination or target device, address of originating device, length of packet, etc. 2. Text or payload – the data to be transmitted... 3. Trailer – end of packet, and error detection and correction bits..." Therefore, the Cheney reference(s) clearly indicate(s) that the secondary set of control signals from the compressed transport stream's control signals indicates at least a first byte of a transport stream packet to be stored in the frame buffer, a first byte of the transport stream packet and a last byte of the transport steam packet, which are required in order to process the transport stream packets/frames and store the packets/frames in a frame buffer memory.

As to claim 25, the claim is rejected based on the rejection of claims 14 and 24.

5. Claims 18-20 are also rejected under 35 U.S.C. 103(a) as being unpatentable over Schindler et al (USPN 5,900,867), in view of So (USPN 5,909,559), both cited by the Examiner.

As to claim 18, the Schindler et al reference discloses a system for receiving a digital video broadcast signal. The claimed "tuner to receive a digital broadcast signal and to provide an analog output signal" is met by tuner 410 in Fig. 4, which receives a digital signal (MPEG or MPEG-2) that is transmitted on an analog carrier signal (see col. 10, lines 31-40). The claimed "demodulator coupled to...the tuner, and to provide a transport stream" is met by digital demodulator 412, which demodulates the tuned signal and provides the compressed digital MPEG transport stream signals (col. 10, lines 37-44 and 51-56). The claimed "video graphics adapter..." is met in part by the video graphics adapter (VGA) 318, as shown in Fig. 5, where the controller 510 or tuner 526 and/or decoder 530 send the MPEG encoded video stream to the MPEG-2 decoder 512 (col. 11, line 34 – col. 12, line 18). The claimed "video graphics adapter

further includes a bus interface port coupleable to a central processing unit" is met by the PCI bus interface port from controller 510 in VGA card 318 (see Fig. 5 and col. 11, lines 35-38), which is coupleable to processor 310 via the PCI Bus (see Fig. 3 and col. 9, lines 17-24). The claimed VGA further includes an engine, or graphics engine is met by the MPEG-2 decoder 512 in Fig. 5 (see col. 11, lines 37-44), and the claimed video output port is met by either the audio video output connector 542 (see col. 11, lines 61-63 and col. 12, lines 3-6), or the video output 522 as shown in Fig. 5 (see col. 11, lines 40-55, more specifically lines 52-55). The Schindler et al reference teaches that the digital video broadcast signal as described above is transmitted through the PCI bus 312. Schindler also teaches that the VGA 318 as shown in Fig. 5 may also directly receive broadcast signals through audio and video inputs 524, 544, 546 and 548 (col. 11, lines 56-66), more specifically, standard cable connector 524, which may receive broadcasts, is coupled to tuner circuit 526 (col. 11, lines 56-60). Although the Schindler et al reference does not explicitly disclose that the video broadcast received through connector 524 is a digital video broadcast, and more specifically the claimed, "transport stream port to receive the compressed transport stream and another transport stream", the So reference teaches improved integrated circuits and computer system embodiments for desktop and computers, television sets, set-top boxes and appliances improved with asymmetrical multiprocessors (see col. 129, lines 22-37). More specifically, the So reference teaches the use of a multimedia system with multiple buses, including a PCI bus or bus 124 in Fig. 1 (330 in later Figs.), as well as the claimed, "transport stream port to receive the compressed transport stream and another transport stream" as met by the north bridge chip 108, which has multiple ports and a PCI or system bus connection through the PCI port to the PCI/system bus 124/330 (see Figs. 1 and 126-127 and col. 129, line 23 – col.

131, line 30). Multiple transport streams may be received through the 1394 port and/or TV tuner 130. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the method of receiving video graphics data as disclosed by the Schindler et al reference with the teachings the So reference which discloses using a north bridge integrated interface for multiple buses in conjunction with the frame buffer memory and a system or PCI bus for the advantage of having the ability to receive various types of broadcasts or multimedia streams through a computer system with a video graphics adapter or graphics engine and bus type system, in addition to providing the advantages of reducing hardware components, simplifying the system and bypassing the PCI bus, which would cut manufacturing costs and improve processing speed as shown by the So reference. One of ordinary skill in the art would have been led to make such a modification since television/multimedia receivers used with computers are well known in the art to provide additional capabilities within a computer system and combining the components in to a single system before connecting to the PCI bus as shown by the So reference would provide a more efficient system.

As to claim 19, the Schindler reference discloses a memory to store at least a portion of the compressed transport stream as met by DRAM 514 in Fig. 5 (see col. 11, lines 37-47). More specifically, the So reference as combined above with Schindler further teaches an internal memory 128 or frame buffer memory (DRAM) coupled to the graphics engine 126, the transport stream port (116 of DSP1), and the system bus interface port (PCI 122) to store at least a portion of the transport stream... as previously described above in claim 14.

As to claim 20, the Schindler reference discloses the claimed central processor unit coupled to the bus interface port of the video graphics adapter as met by processor 310 (see Fig.

3 and col. 9, lines 17-24), which is coupled to the bus interface port (controller 510) of the VGA 318 via the PCI BUS 312 (see Fig. 5 and col. 11, lines 35-38). The claimed transport demultiplexer coupled to the demodulator is met by the demultiplexer 416, which is coupled to the demodulator 412 through the F.E.C. 414 as shown in Fig. 4 (see col. 10, lines 40-58).

6. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schindler et al (USPN 5,900,867), in view of Malladi et al (USPN 5,912,676), and in further view of Datari (USPN 6,418,169), all cited by the Examiner.

As to claim 21, note the Schindler et al reference which discloses a method of storing video data. Schindler et al discloses multiple modes of operation, such as receiving a digital video broadcast signal (MPEG/compressed) from a satellite dish as shown in Fig. 4, or receiving a standard cable broadcast signal at 524 as shown in Fig. 5. The claimed first mode of operation comprising storing pixel information in a frame buffer of a video adapter, wherein one line of frame buffer memory is representative of one line of a video image to be displayed is met in part by receiving an uncompressed signal from a cable video source through connector 524 (Fig. 5), as described above, where the video signal may be buffered in VRAM 518 for output to a monitor (see col. 11, line 34 – col. 12, line 3). Although, Schindler does not explicitly disclose that one line of the frame buffer memory is representative of a line of video image to be displayed, it is well known in the art of uncompressed video frame buffers that a line of frame buffer memory may be *representative* of a line of a video image to be displayed. The Malladi et al reference teaches that various frame storage formats exist for storing frame data in memory, and that one method for storing a frame of pixel data is on a scan line basis, where the data is

stored in memory scan line by scan line for pictures or frames that are to be displayed (see col. 4, lines 30-37). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the method of the Schindler et al reference which discloses multiple modes of operation and storing video data, with the Malladi et al reference, which specifically teaches that one line of frame buffer memory may be representative of one line of a video image to be displayed for the advantage of providing a storage format which provides improved or optimum performance for storing a reference frame of pixel data on a scan line basis. The claimed second mode of operation comprising storing compressed transport stream data in the frame buffer, wherein one line of frame buffer memory is representative of one transport stream packet is met in part by the Schindler et al reference, which also discloses receiving an MPEG transport stream from a digital video source Fig 4, as described above, where the compressed MPEG transport stream is sent to the PCI bus 312, where the video graphics adapter card receives the MPEG stream through controller 510 (Fig. 5, col. 11, lines 34-37), and the MPEG data is routed to MPEG-2 decoder 512 with associated random access memory (DRAM 514), which is used as buffer in assisting with the decoding (see col. 11, lines 37-47) and in lines 34-52 (specifically lines 49-52), the MPEG data (compressed video) may be provided back to controller 510, which then places the video information into dynamic random access memory (DRAM) or video random access memory (VRAM) **518** as used by the other video signal described above. The **VRAM 518** is a frame buffer which buffers the video before it is transmitted for display. Although, the Schindler et al reference does not explicitly disclose that one line of the frame buffer memory is representative of one transport stream packet, it is well known in the art of video transport streams that are stored in frame buffers that a MPEG-2

transport stream packet has a fixed 188 byte length as defined by MPEG standards, and therefore, a line of frame buffer memory is *representative* of a transport stream packet since every MPEG-2 transport stream packet has already been produced and transmitted according to the established MPEG standards so that when received by a frame buffer memory a line of memory is representative of one transport stream packet. In addition to, the Datari reference teaches that MPEG video data packets may be stored or buffered in memory and sequentially accessed by priority (see col. 5, lines 13-42 and col. 6, lines 62-66, also see col. 8, lines 10-18). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further combined the method of Schindler et al which discloses multiple modes of operation and storing video data, with the Datari reference, which specifically teaches that a line of the frame buffer memory may be representative of one MPEG or transport stream packet for the advantage of providing a storage format which allows for improved priority accessing of transport stream packets of video images to be displayed.

Allowable Subject Matter

7. Claims 2-13 and 22-23 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

As to independent claim 22, the prior art, alone or in combination, does not teach or fairly suggest a video graphics system comprising all of the claimed subject matter in it's entirety including a data storage controller having at least one pair of a plurality of internal control ports to communicate control signals within the data storage controller.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Auld et al. (USPN 6,526,583) – Discloses a unified memory architecture.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael W. Hoye whose telephone number is **571-272-7346**. The examiner can normally be reached on Monday to Friday from 8:30 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller, can be reached at **571-272-7353**.

Any response to this action should be mailed to:

Please address mail to be delivered by the United States Postal Service (USPS) as follows:

Mail Stop _____
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Except correspondence for Maintenance Fee payments, Deposit Account Replenishments (see 1.25(c)(4)), and Licensing and Review (see 37 CFR 5.1(c) and 5.2(c)), please address correspondence to be delivered by other delivery services (Federal Express (Fed Ex), UPS, DHL, Laser, Action, Purolater, etc.) as follows:

United States Patent and Trademark Office
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Some correspondence may be submitted electronically. See the Office's Internet Web site **http://www.uspto.gov** for additional information.

Or faxed to: 571-273-8300

Hand-delivered responses should be brought to the Customer Service Window at the address listed above.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to customer service whose telephone number is **571-272-2600**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see **http://pair-direct.uspto.gov**. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at **866-217-9197** (toll-free).

Michael W. Hoye
August 6, 2007

ANDREW Y. KOENIG
PRIMARY PATENT EXAMINER